What is claimed is:

1. An electrostatic discharge (ESD) protection circuit comprising:

an NMOS transistor connected between an input/output pad and a ground, the NMOS transistor having a parasitic bipolar transistor; and

at least one diode connected between the input/output pad and the NMOS transistor.

2. The ESD protection circuit of claim 1, wherein

an output terminal of the diode is connected to a base of the parasitic bipolar transistor.

3. The ESD protection circuit of claim 1, wherein

the diode is a PN diode.

4. The ESD protection circuit of claim 1, wherein the at least one diode includes a plurality of N diodes.

5. The ESD protection circuit of claim 1, wherein

the at least one diode includes a plurality of N diodes, and

a count of the diodes N of the plurality of N diodes is determined so as to stop a current flow through the at least one diode during a normal operation of a chip.

6. The ESD protection circuit of claim 4, wherein, the plurality of N diodes are connected in series to each other in a forward direction.

7. The ESD protection circuit of claim 4, wherein

p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively,

the second diode through the N-1 diode of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode, and

an n+ junction of an N diode is connected to the substrate.

8. An electrostatic discharge (ESD) protection circuit comprising:

an input/output pad;

a plurality of N diodes connected in series between the input/output pad and a substrate of an NMOS transistor; and

the NMOS transistor is connected between the input/output pad and has a parasitic bipolar transistor connected to the plurality of N diodes.

9. The ESD protection circuit of claim 8, wherein

the substrate is a p-type substrate and connected to a ground.

10. The ESD protection circuit of claim 8, wherein

the plurality of N diodes are PN diodes.

11. The ESD protection circuit of claim 8, wherein a number of N diodes in the plurality of N diodes is determined so as to stop a current flow through the plurality of N diodes during a normal operation of a chip.

12. The ESD protection circuit of claim 8, wherein

p+ and n+ junctions of a first diode of the plurality of N diodes are connected to the input/output pad and a p+ junction of a second diode of the plurality of N diodes, respectively,

the second diode through the N-1 diodes of the plurality of N diodes are connected such that an n+ junction of each of the second diode through the N-1 diode is connected to the p+ junction of a subsequent diode; and

an n+ junction of an N diode is connected to the substrate.

13. The ESD protection circuit of claim 8, wherein the output terminal from the Nth diode of the plurality of N diodes is connected to the base of the parasitic bipolar transistor.

14. An electrostatic discharge (ESD) protection circuit comprising:

an input/output pad;

at least two diodes connected in parallel between the input/output pad and a substrate of an NMOS transistor; and

the NMOS transistor is connected between the input/output pad and has a parasitic bipolar transistor connected to the plurality of N diodes.

15. The ESD protection circuit of claim 8, wherein
the substrate is a p-type substrate and connected to a ground.

16. The ESD protection circuit of claim 8, wherein
the diodes are PN diodes.